REMARKS

Claims 21-26 are in the present application.

The Examiner objected to the limitation "perpendicularly to word lines" in claims 21 and 24 on pages 23 and 24 on line 10 as having insufficient antecedent basis. The Examiner also objected to the limitation "extending in parallel with said word lines" in claim 21 on line 19 as having insufficient antecedent basis.

Claim 21(a) has been amended by adding "with one another and perpendicular to a plurality of word lines" to add the necessary antecedent basis.

Claim 21(c) has been amended by adding "said plurality of" before word lines because there is now antecedent basis for "word lines."

Claim 24(a) has been amended by adding "with one another and perpendicular to a plurality of word lines" to add the necessary antecedent basis.

Claim 24(c) has been amended by adding "said plurality of" before word lines because there is now antecedent basis for "word lines."

The Examiner objected to the term "extended bit line" in claim 21 as having a meaning repugnant to the usual meaning of that term. The Examiner also objected to the term "extended source line" in claim 24 as having a meaning repugnant to the usual meaning of that term.

Claim 21(h) has been amended to replace the term "extended bit line" with "plurality of bit studs."

Claim 24(h) has been amended to replace the term "extended source line" with "plurality of source studs."

It is submitted that all of Applicants' claims are now in full compliance with the provisions of 35 U.S.C. 112.

In paragraph 6 of the outstanding Office Action claim 21 stands rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya, et al. (U.S. Patent No. 5,838,615) in view of Kim (U.S. Patent No. 5,834,807). However, it is believed that the Examiner intended to also reject claims 22 and 24 as unpatentable over Kamiya in view of Kim since these additional two claims are also discussed in paragraph 6. The Applicants will treat the rejection accordingly.

Claim 21(j) has been amended to read "forming a second metal wiring layer which is patterned so as to form a bit line extending perpendicularly to said word lines and connecting said drain regions with each other, said bit line having a top portion and a bottom portion with said top portion being wider than said bottom portion, wherein said bottom portion of said bit line is connected to said top portion of said plurality of bit studs and said bottom portion of said plurality of bit studs is connected to said drain regions."

The amendment to claim 21(j) was made to clearly show that the bit line (15a) of the present invention, shown in Applicants' FIG. 11E, comprises two portions, a top portion and a bottom portion, with the top portion being wider than the bottom portion. The bottom portion of the bit line (15a) is connected to the top portion of the plurality of bit studs (12b) in FIG. 11E. The bottom portion of the plurality of bit studs (12b) is connected directly to the drain regions (8a) in FIG. 11E.

In contrast, Kamiya teaches a single portion bit line (118a), shown in FIG. 7., the bottom of which contacts the tungsten film (115) that is connected to drain diffusion layer (109a). Kamiya does not disclose a bit line with two portions, a top portion and a bottom portion, the top portion being wider than the bottom portion, as recited by Applicants. Kim teaches a bit line (80), in FIG. 8G, which contacts a pad layer (73). The pad layer (73) then contacts an intermediate plugged conductive layer (69). The intermediate plugged conductive layer (69) then contacts an N-type high concentration impurity layer (58). Kim does not teach a plurality of bit studs and a bit line, the bottom portion of the bit line being connected to the top portion of the plurality of bit studs, the bottom portion of the plurality of bit studs being connected directly to the drain regions, as recited by Applicants.

Therefore, the Patent and Trademark Office does not make out a prima facie case of obviousness under 35 U.S.C. 103(a).

Because claim 21 is believed to be allowable over Kamiya in view of Kim, claim 22 is also believed to be allowable since it depends from claim 21.

Claim 24(h) has been amended to read "forming a first metal wiring layer which is patterned so as to form both a bit line connecting said drain regions to one another, and a plurality of source studs extending in parallel with said word lines, said plurality of source studs connecting to said source regions, said plurality of source studs having a top portion and a bottom portion with said top portion of said plurality of source studs being wider than said bottom portion of said plurality of source studs."

Claim 24(h) has been amended to clearly show that the plurality of source studs (12d) of the present invention, shown in Applicants' FIG. 15, comprises two portions, a top portion and a bottom portion, the top portion being wider than the bottom portion. The top portion of the plurality of source studs (12d) contacts the bottom portion of the common source line (15b) in FIG. 15. Also, the present invention forms both the bit line and the plurality of source studs from the same first metal wiring layer, the plurality of source studs directly contacting the source regions.

In contrast, Kim teaches a single portion common source line (71), shown in FIG. 8G, that is connected to the source regions through an intermediate plugged conductive layer (66) that was formed in a previous step. Kim does not teach a plurality of source studs and a common source line, the bottom portion of the common source line being connected to the top portion of the plurality of source studs, the bottom portion of the plurality of source studs being connected directly to the source regions, as recited by Applicants. Kamiya also teaches a single portion common source line (118b), shown in FIG. 7. Kamiya does not teach a common source line which comprises two portions, a top portion and a bottom portion, the top portion being wider than the bottom portion, as recited by Applicants.

Therefore, the Patent and Trademark Office does not make out a prima facie case of obviousness under 35 U.S.C. 103(a).

Claim 24(j) has been amended to read "forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other, said common source line having a top portion and a bottom portion with said top portion of said common source line being wider than said bottom portion of said common source line, wherein said bottom portion of said common source line is connected to said top portion of said plurality of source studs and said bottom portion of said plurality of source studs is connected to said source regions."

Claim 24(j) has been amended to clearly show that the common source line (15b) of the present invention, shown in FIG. 15, comprises two portions, a top portion and a bottom portion, the bottom portion contacting the top portion of plurality of source studs (12d). The bottom portion of the plurality of source studs (12d) is, in turn, connected directly to the source regions (8b).

In contrast, Kamiya teaches a single portion common source line (118b), shown in FIG. 7. Kamiya does not teach a common source line which comprises two portions, a top portion and a bottom portion, the top portion being wider than the bottom portion, as recited by Applicants. Kim teaches a bit line (80), shown in FIG. 8G, formed from a second metal wiring layer that is connected to the drain regions through both a pad layer (73) formed from the first metal wiring layer and an intermediate plugged conductive layer (66) that was formed in a step prior to the forming of the first metal wiring layer. Kim does not teach a plurality of source studs and a common source line, the bottom portion of the common source line being connected to the top portion of the plurality of source studs, the bottom portion of the plurality of source studs being connected directly to the source regions, as recited by Applicants.

Therefore, the Patent and Trademark Office does not make out a prima facie case of obviousness under 35 U.S.C. 103(a).

In paragraph 7 of the outstanding Office Action claim 23 stands rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya in view of Kim as applied to claim 21 above, and in further view of Yonemoto (U.S. Patent No. 5,506,434).

Because claim 21 is believed to be allowable over Kamiya in view of Kim, claim 23 is also believed to be allowable since it depends from claim 21. Yonemoto does not teach

the first and second metal wiring layer structures as recited by applicant and is therefore irrelevant.

In paragraph 8 of the outstanding Office Action claims 25 and 26 stand rejected under 35 U.S.C. 103(a) as unpatentable over Kamiya in view of Kim as applied to claim 24 above, and in further view of Cacharelis, et al. (U.S. Patent No. 5,550,072).

Because claim 24 is believed to be allowable over Kamiya in view of Kim, claims 25 and 26 are also believed to be allowable since they depend from claim 24. Cacharelis does not teach the first and second metal wiring layer structures as recited by applicant and is therefore irrelevant.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance. Reexamination and reconsideration of the application, as amended, and allowance of the claims at an early date is respectfully requested.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.:	09/606,159	Group Art Unit:	2815
Filed:	6/29/00	Docket No.:	037267-0135
Title:	EEPROM SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME		

MARK-UP COPY OF SPECIFICATION IN REPLY TO OFFICE ACTION MAILED JANUARY 4, 2001

IN THE SPECIFICATION:

On page 1, line 29, replace the paragraph as follows:

As illustrated in Fig. 3A, a p-type well 2 is formed in a p-type semiconductor substrate 1 in a region where a memory cell array is to be formed. Then, a plurality of field insulating films 3 is formed in the form of islands by selective oxidation. The field insulating films are not illustrated ~~only~~ in Fig. 3A, but are insulated in Fig. 2.

On page 3, line 25, replace the paragraph as follows:

As a result, as illustrated in Fig. 4 which is a cross-sectional view taken along the line IV-IV in Fig. 1, there is formed an undesirable recess 19 at a surface of the semiconductor substrate 1. The undesirable recess 19 causes junction leakage therein, which ~~pauses~~ poses a problem that data-writing and data-eliminating properties are deteriorated.

On page 4, line 20, replace the paragraph as follows:

As illustrated in Fig. 8A, a p-type well 2 is formed in a p-type semiconductor substrate 1 by introducing p-type impurities into the semiconductor substrate 1 and thermally diffusing the p-type impurities and the semiconductor substrate 1. Then, a plurality of field insulating films 3 are formed on a principal surface of the p-type well 2 by selective oxidation so that the field insulating films 3 extend in parallel with one another, but perpendicularly to word lines which will be formed later. The field insulating films 3 are not illustrated ~~only~~ in Fig. 8A, but are illustrated in Fig. 5.

On page 6, line 23, replace the paragraph as follows:

In accordance with the above-mentioned method, when the first polysilicon layer 5a is etched, the thick field insulating films 3 exist below a region to be etched. When

the second and first polysilicon layers 7a and 5a are patterned to thereby form the control gate 7 and the floating gate 5, a region where only a single polysilicon layer is etched is a region located above the field insulating regions 3. Hence, the above-mentioned undesirable recess 19 caused by etching a polysilicon layer is not formed. Accordingly, there is solved a problem that junction leakage ~~junction leakage~~ occurs due to the recess, and resultingly data-writing and data-eliminating properties are deteriorated, and that a fabrication yield due to the breakage in a source region is reduced.

On page 13, line 12, replace the paragraph as follows:

Then, a plurality of field insulating films 3 composed of silicon dioxide are formed in parallel by selective oxidation. The field insulating films 3 extend perpendicularly to word lines which will be formed later, and have a thickness in the range of 4000 to 8000 angstroms. The field insulting films 3 are not illustrated ~~only~~ in Fig. 11A, but are illustrated in Fig. 10.

IN THE CLAIMS:

21. (Amended) A method of fabricating an EEPROM semiconductor device, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and perpendicular to a plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon layers in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said first polysilicon layer to thereby form a control gate and a floating gate;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

[(h) forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said word lines and connecting source regions to one another and an extended bit line connecting said drain region to a bit line;]

(h) forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said word lines and connecting source regions to one another and a plurality of bit studs extending to said drain regions;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

[(j) forming a second metal wiring layer which is patterned so as to form a bit line connecting said drain regions to one another.]

(j) forming a second metal wiring layer which is patterned so as to form a bit line extending perpendicularly to said word lines and connecting said drain regions with each other, said bit line having a top portion and a bottom portion with said top portion being wider than said bottom portion,

wherein said bottom portion of said bit line is connected to said top portion of said plurality of bit studs and said bottom portion of said plurality of bit studs is connected to said drain regions.

24. (Amended) A method of fabricating an EEPROM semiconductor device, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and perpendicular to a plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon layers in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said first polysilicon layer to thereby form a control gate and a floating gate;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

[(h) forming a first metal wiring layer which is patterned so as to form both a bit line extending almost in parallel with said field insulating films and connecting drain regions to one another, and an extended common source line connecting said source region to a later mentioned common source line;]

(h) forming a first metal wiring layer which is patterned so as to form both a bit line connecting said drain regions to one another, and a plurality of source studs extending in parallel with said word lines, said plurality of source studs connecting to said source regions, said plurality of source studs having a top portion and a bottom portion with said top portion of said plurality of source studs being wider than said bottom portion of said plurality of source studs;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

[(j) forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions to one another.]

(j) forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other, said common source line having a top portion and a bottom portion with said top portion of said common source line being wider than said bottom portion of said common source line,

wherein said bottom portion of said common source line is connected to said top portion of said plurality of source studs and said bottom portion of said plurality of source studs is connected to said source regions.